

REMARKS

Reconsideration of the present application is requested. Claims 1-44 are currently pending. Claims 1, 40 and 41-44 are independent claims.

PRIOR ART REJECTIONS

§ 102 Rejection – Koshiishi

Claim 44 stands rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,919,332 ("*Koshiishi*"). This rejection is respectfully traversed.

I. The shape of the insulating plate is a structural feature, but not intended use.

The Examiner believes that the recitation of, "the insulating plate being shaped so as to guide gas away from a center portion of a semiconductor wafer," is an intended use of the apparatus of claim 44. U.S. Pat. & Trademark Office, Final Office Action for Appl. Ser. No. 10/762,526, p. 5 (November 16, 2007) Applicants disagree.

As clearly stated in claim 44, the insulating plate is, "*shaped* so as to guide gas away from a center portion of the semiconductor wafer." A *shape* of an insulating plate is clearly structural, not intended use. Therefore, this feature of claim 44 should be given patentable weight.

If the Examiner remains unconvinced, Applicants respectfully request the Examiner provide some explanation as to how the shape of the insulating plate of claim 44 is intended use, but not a structural feature.

II. Koshiishi fails to anticipate claim 44.

As previously argued, *Koshiishi* fails to teach or fairly suggest all features of the insulating plate of claim 44. In FIG. 1 of *Koshiishi*, processing gas is supplied through diffusion holes 22 above the center portion of the wafer W. *Koshiishi* at 10:19 – 10:25. The insulating member 31 is arranged to, "cover the outer circumferential lower edge of the upper electrode 21," (*Id.* at 10:29-10:31) and insulate the upper electrode 21 and the processing container 3 (*Id.* at 10:25-10:28). The insulating member 31 of *Koshiishi* is also arranged such that a narrow gas flow path is formed between the lower surface of the insulating member 31 and upper edge 13a of the lower insulating member 13. *Id.* at 10:40-10:43. Thus, in the context of *Koshiishi*, the insulating member 31 is, at most, shaped to guide gas *toward* the center portion of the wafer W, but not "to guide gas *away* from a center portion of the semiconductor wafer," as required by claim 44.

For at least this reason, claim 44 is patentable over *Koshiishi*.

§ 102 Rejection – Fujimoto

The Examiner further rejects claim 44 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,413,673 ("*Fujimoto*"). This rejection is respectfully traversed.

I. The shape of the insulating plate is a structural feature, but not intended use.

For the reasons discussed above, the recitation of "the insulating plate being shaped so as to guide gas away from a center portion of a semiconductor

wafer," in claim 44 is clearly structural, not intended use. Therefore, this feature of claim 44 should be given patentable weight.

II. Fujimoto fails to anticipate claim 44.

In *Fujimoto*, gas is introduced through gas pipe 60 arranged above the center portion of the workpiece 50. *See, e.g., FIG. 5B*. Dielectric spacers 42 are provided on both upper electrode 1 and the lower electrode 52. *Id.* The dielectric spacers 42 extend toward each other such that the vertical distance between the upper and lower dielectric spacer is less than the distance between upper electrode 1 and the lower electrode 52. *Id.* Thus, in the context of *Fujimoto*, the dielectric spacers 42 are at most shaped so as to guide gas *toward* the central portion of the wafer 50, but *not* "to guide gas away from a center portion of a semiconductor wafer," as in claim 44. *See, Fujimoto* at col. 4, ll. 45 – 67 and col. 5, ll. 1-3 (*referring* to the function of the spacer 41 in FIG. 5A, which has the same functionality as the spacer 42 in FIG. 5B).

For at least this reason, claim 44 is patentable over *Fujimoto*.

§ 102 Rejection – Berman

Claim 44 is also rejected under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent No. 6,837,967 ("*Berman*"). This rejection is respectfully traversed.

I. The shape of the insulating plate is a structural feature, but not intended use.

For the reasons discussed above, the recitation of "the insulating plate being shaped so as to guide gas away from a center portion of a semiconductor

wafer," in claim 44 is clearly structural, not intended use. Therefore, this feature of claim 44 should be given patentable weight.

II. *Berman* fails to anticipate claim 44.

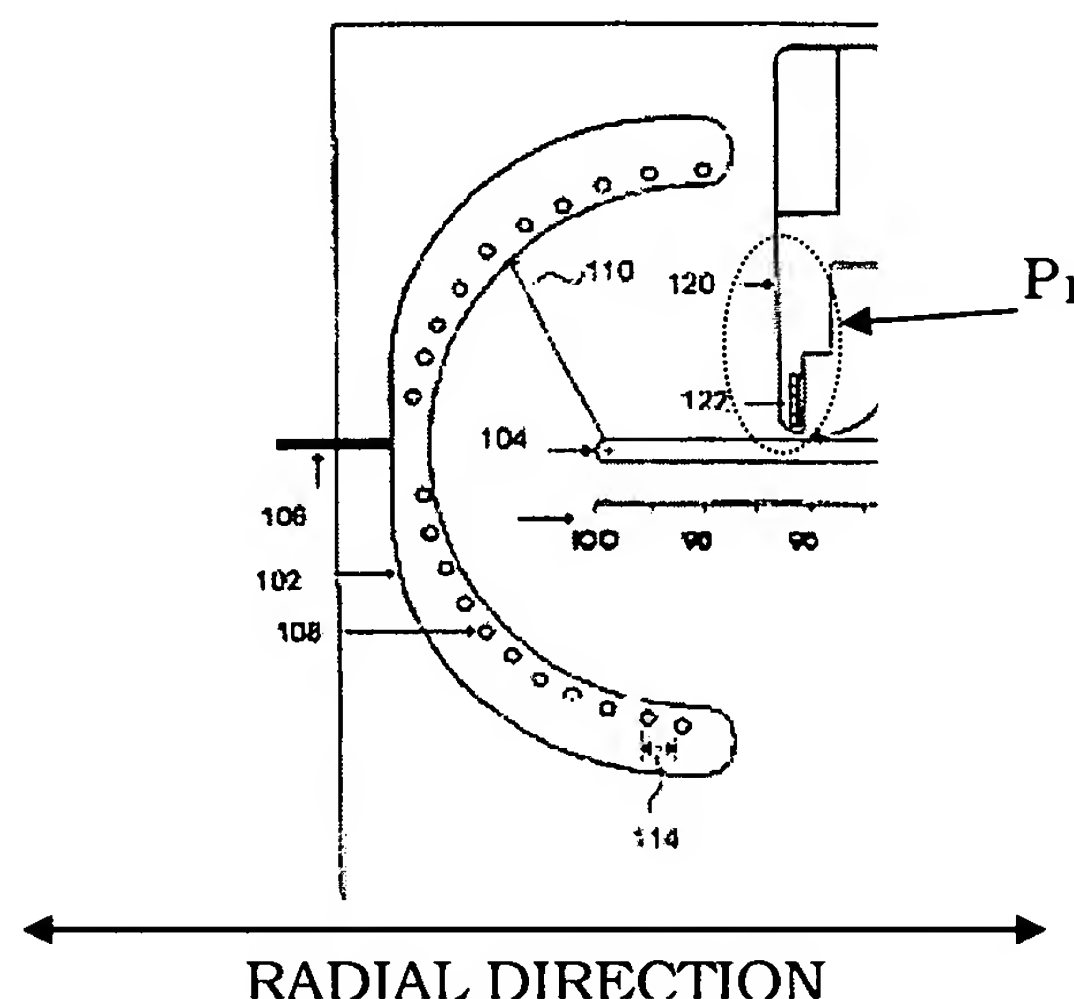
On page 5 of the Final Office Action, the Examiner dismisses Applicants' argument that FIGS. 2A-2D of *Berman* fail to teach or suggest the "insulating plate," of claim 44. In doing so, the Examiner directs Applicants attention instead to FIG. 1 of *Berman*. However, FIG. 1 of *Berman*, also fails to teach or suggest an insulating plate including, *inter alia*, "a protrusion, including a sloped surface and a cliff surface, the protrusion protruding outwardly in a direction parallel to a radial direction of the body," as required by claim 44.

As shown in FIG. 1 of *Berman* (the relevant portion of which is reproduced below for the Examiner's convenience), cylindrically shaped top plate 120 has a plasma confining top magnetic coil 122 located at its periphery. *Berman* at col. 5, ll. 58 – 60 and col. 6, ll. 25-27. The portion of the top plate 120 including the top magnetic coil 122 extends vertically downward toward the wafer 104. *See, e.g.*, FIG. 1.

Contrary to the insulating plate of claim 44, however, the protruding portion of the top plate 120 including the top magnetic coil 122 (identified as P₁ in the portion of FIG. 1 shown below) does not include any "sloped surface." As noted above, this portion of the top plate 120 extends *vertically downward*. *See, Berman* at FIG. 1.

Moreover, the portion of the top plate 120 including the magnetic coil 122 protrudes in a direction *perpendicular* to a radial direction (also know as

axial direction) of the top plate 120, but not "outwardly in a direction *parallel* to a radial direction," of the top plate 120, as required by claim 44, assuming *arguendo* that the top plate 120 corresponds to the "body," of claim 44 (which Applicants do not admit).



For at least the foregoing reasons, *Berman* does not anticipate claim 44.

REJECTION UNDER 35 U.S.C. § 103(a)

The Examiner rejects claims 1-8 and 10-39 under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent Application Publication No. 2003/0150562 ("*Quon*") in view of *Berman*. This rejection is respectfully traversed.

Claim 1 is directed to an apparatus for etching an edge of a semiconductor wafer. The apparatus includes a bottom electrode arranged below the semiconductor wafer and acting as a stage to support the semiconductor wafer. An upper electrode is arranged above the semiconductor wafer. An insulating plate is arranged adjacent to the upper electrode with a

gap there between. The insulating plate is configured such that only an edge portion of the upper electrode is exposed to the bottom electrode.

The apparatus of claim 1 is not rendered obvious by *Quon* and/or *Berman*, taken singly or in combination, at least because neither reference discloses or fairly suggests an insulating plate, "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode."

The Examiner relies upon the ceramic washer 80 to allegedly teach the "insulating plate," of claim 1, but appears to correctly recognize that *Quon* does not teach or suggest an insulating plate, "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode," as required by claim 1. The Examiner relies upon *Berman* to teach this feature.

Applicants disagree with this conclusion, and to be thorough, Applicants will discuss each of *Quon* and *Berman* in turn.¹

As shown in FIG. 1 of *Quon* (which is shown below), the entire surface of the upper electrode 10 is exposed to the bottom electrode 20. Moreover, a quartz shield ring 13 and a chuck focus ring 15 are situated such that the upper edge electrode 30 and the lower edge electrode 40 are not exposed to one another at all. *See, e.g., Quon* at FIG. 1. Thus, *Quon* does not disclose an insulating plate, "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode," as required by claim 1.

¹ For the sake of clarity, Applicants provide discussions of each of the references separately, however, Applicants are not attacking these references individually, but arguing that the references, even taken in combination, fail to render the claimed invention obvious because all features of claim 1 are not found in the prior art.

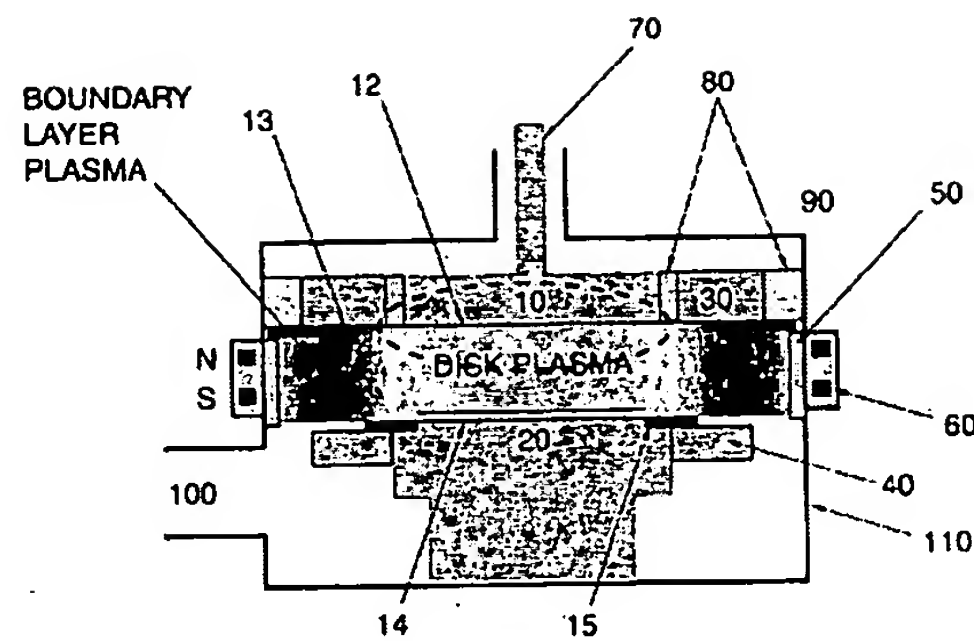


FIG. 1

As noted above, the Examiner appears to correctly recognize that *Quon* does not teach or suggest an insulating plate, "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode," as required by claim 1, but relies upon the top plate 120 of *Berman* to allegedly teach this feature. The top plate 120 of *Berman*, however, is not "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode," as required by claim 1, and thus, does not constitute the insulating plate of claim 1.

As shown in FIG. 1 of *Berman*, the top plate 120 does not impede or prohibit exposure of an upper portion of the electrode 102 to a lower portion of the electrode 102. In fact, the top plate 120 is not situated between upper and lower portions of the electrode 102. Therefore, the top plate 120 of *Berman* is not "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode," as required by claim 1.

Moreover, at most, only the wafer 104 (when present) is situated between an upper portion and lower portion of the electrode 102. But, as both the

Examiner and one of ordinary skill will surely appreciate, the wafer 104 is not an insulating plate, and thus, does not constitute the "insulating plate," of claim 1.

For at least the foregoing reasons, *Berman* fails to teach or suggest an insulating plate, "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode," as required by claim 1.

Because an insulating plate, "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode," as required by claim 1, is absent from both *Quon* and *Berman*, the combination of references (assuming such a combination could be made) does not render claim 1 obvious.² Claims 2-8 and 10-39 are not anticipated nor rendered obvious by *Quon* or *Berman*, taken singly or in combination, at least by virtue of their dependency.

The above notwithstanding, even assuming *arguendo* that *Berman* did disclose an insulating plate, "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode," as required by claim 1 (which Applicants do not admit for at least the reasons set forth above), one of ordinary skill would not have combined *Quon* and *Berman* because such a combination would change the principal operation of *Quon*. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

² Again, for the sake of clarity, Applicants provide discussions of each of the references separately, however, Applicants are not attacking these references individually, but arguing that the references, even taken in combination, fail to render the claimed invention obvious because all features of claim 1 are not found in the prior art.

As discussed above, the entire surface of the upper electrode 10 is exposed to the bottom electrode 20. See, *Quon* at FIG. 1. Moreover, a quartz shield ring 13 and a chuck focus ring 15 are situated such that the upper edge electrode 30 and the lower edge electrode 40 are not exposed to one another at all. See, e.g., *Quon* at FIG. 1. Thus, if *Quon* was modified to include an insulating plate, "configured such that only an edge portion of the upper electrode is exposed to the bottom electrode," as required by claim 1, the entire upper electrode 10 would no longer be exposed to the bottom electrode 20 and/or the upper edge electrode 30 would no longer be shielded from the lower edge electrode 40 (as is the case in FIG. 1 of *Quon*).

For at least the foregoing reasons, withdrawal of this rejection is requested.

Rejection of claim 9

The Examiner further rejects claim 9 under 35 U.S.C. § 103(a) as allegedly unpatentable over *Quon*, in view of *Berman* and further in view of U.S. Patent Application Publication No. 2003/0201069 ("*Johnson*"). This rejection is respectfully traversed.

Applicants respectfully assert that this rejection has been overcome by overcoming the above-described rejection of independent claim 1. Accordingly, reconsideration of this rejection and allowance of each of dependent claim 9 is respectfully requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-44 in connection with the present application is earnestly solicited.

Pursuant to 37 C.F.R. §§ 1.17 and 1.136(a), applicant hereby petitions for a three (3) month extension of time for filing a reply to the outstanding Office Action and submit the required \$1,050.00 extension fee herewith.

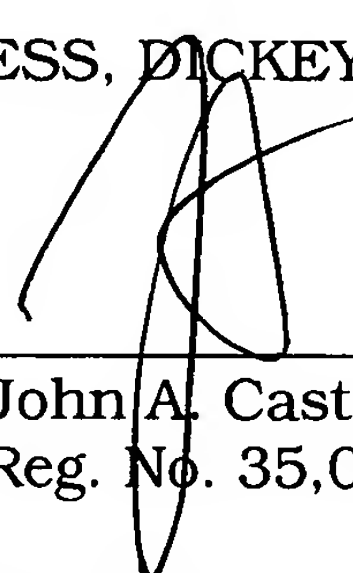
If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKY & PIERCE, PLC

By


John A. Castellano
Reg. No. 35,094

JAC/AMW:krm



P.O. Box 8910
Reston, VA 20195
(703) 668-8000